

**S/N 09/820,898**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Girish P. Ramanathan et al.

Examiner: Thuan Du

Serial No.: 09/820,898

Group Art Unit: 2116

Filed: March 30, 2001

Docket No: 884.963US1

Title: SYSTEM FOR VARYING TIMING BETWEEN SOURCE AND DATA  
SIGNALS IN A SOURCE SYNCHRONOUS INTERFACE

Assignee: Intel Corporation

Customer No: 21186

**SUPPLEMENTAL AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**RECEIVED**

JUL 27 2004

Technology Center 2100

Please amend the above-identified patent application as follows:

**SUPPLEMENTAL AMENDMENT**

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**IN THE DRAWINGS**

Please substitute the new FIG. 2 for the previous FIG. 2 in its entirety. In FIG. 2, block 4, entitled "STBSYNC", the identifier "4" has been replaced with "24". This change is made to be consistent with references made in the text of the Detailed Description. This particular identifier is referenced in the Detailed Description on page 8, lines 22-23, "In a similar fashion, STBSYNC element 24 also receives the SCK signal as well as the 66 MHz signal." There is no reference, however, anywhere in the specification to an element identified as "4" in any diagram. No new matter has been added.